IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION

SAXON INNOVATIONS, LLC	§	
	§	
V.	§	**CIVIL ACTION NO. 6:07-CV-490**
	§	
NOKIA CORP., et al.	§	

MEMORANDUM OPINION AND ORDER

This claim construction opinion construes the disputed terms in U.S. Patent Nos. 5,502,689 ("the '680 Patent"), 5,592,555 ("the '555 patent"), 5,771,394 ("the '394 Patent").[1] In the above-styled cause of action, Plaintiff Saxon Innovations, LLC accuses Defendants LG Electronics Inc., LG Electronics USA Inc., LG Electronics Mobilecomm U.S.A., Inc., Samsung Electronics Co. Ltd, Samsung Electronics America Inc., Samsung Telecommunications America LLC, Palm Incorporated, Research in Motion Ltd, Research In Motion Corporation, Nintendo Co. Ltd, and Nintendo of America (collectively "Defendants") of patent infringement. The parties have submitted a number of claim terms for construction. Saxon has filed an Opening Claim Construction Brief (Doc. No. 250) and a Reply Claim Construction Brief (Doc. No. 281). Defendants have jointly filed a Responsive Claim Construction Brief. (Doc. No. 272.) A *Markman* hearing was held on June 25, 2009. For the reasons stated herein, the Court adopts the constructions set forth below.

CLAIM CONSTRUCTION PRINCIPLES

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312

[1] Saxon also alleges infringement of U.S. Patent No. 5,247,621 ("the '621 Patent"), and the parties have presented terms from the '621 Patent for construction. However, as explained in the Court's Report and Recommendation regarding Defendants' Motion for Summary Judgment of Invalidity of Claim 1 of the '621 Patent, the Court finds that the only claim of the '621 Patent asserted in this case is invalid. Accordingly, the Court will not address the '621 claim terms disputed by the parties.

(Fed. Cir. 2005) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). In claim construction, courts examine the patent's intrinsic evidence to define the patented invention's scope. *See id.*; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Communications Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). This intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *See Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. *Phillips*, 415 F.3d at 1312-13; *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003).

The claims themselves provide substantial guidance in determining the meaning of particular claim terms. *Phillips*, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id*. Other asserted or unasserted claims can also aid in determining the claim's meaning because claim terms are typically used consistently throughout the patent. *Id*. Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314-15.

Claims "must be read in view of the specification, of which they are a part." *Id*. (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id*. (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms, give a claim term a

different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. *Phillips*, 415 F.3d at 1316. While courts must generally impose a "heavy presumption" in favor of the ordinary meaning of claim terms, this presumption can be overcome by statements of "clear disclaimer" expressly indicating "manifest exclusion or restriction." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004); *Brookhill-Wilk 1, LLC v. Intuitive Surgical Inc.*, 334 F.3d 1294, 1301 (Fed. Cir. 2003); *see also Phillips*, 415 F.3d at 1312-13. Further, this "heavy presumption" does not arise when the patentee acts as his own lexicographer and gives a claim term a different meaning than the term would otherwise possess. *See Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1301(Fed. Cir. 2004); *see also Nystrom v. TREX Co.*, 424 F.3d 1136, 1145 (Fed. Cir. 2005). In these situations, the inventor's lexicography governs. *Phillips*, 415 F.3d at 1316.

Also, the specification may resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex, Inc.*, 299 F.3d at 1325. For example, "[a] claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever correct." *Globetrotter Software, Inc. v. Elan Computer Group, Inc.*, 362 F.3d 1367, 1381 (Fed. Cir. 2004). But, "'[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.'" *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323.

The prosecution history is another tool to supply the proper context for claim construction

because a patent applicant may also define a term in prosecuting the patent. *Home Diagnostics, Inc., v. Lifescan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004) ("As in the case of the specification, a patent applicant may define a term in prosecuting a patent."). The doctrine of prosecution disclaimer is well established and prevents a patentee from recapturing through claim interpretation specific meanings disclaimed during the prosecution of the patent. *See Omega Eng'g, Inc. v. Raytek Corp.,* 334 F.3d 1314, 1323 (Fed.Cir.2003). The prosecution history must show that the patentee "clearly and unambiguously" disclaimed or disavowed the proposed interpretation during the patent's prosecution to obtain claim allowance. *Middleton, Inc. v. 3M Co.,* 311 F.3d 1384, 1388 (Fed.Cir.2002). "Indeed, by distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover." *Spectrum Int'l v. Sterilite Corp.,* 164 F.3d 1372, 1378-79 (Fed.Cir.1998). "As a basic principle of claim interpretation, prosecution disclaimer promotes the public notice function of the intrinsic evidence and protects the public's reliance on definitive statements made during prosecution." *Omega Eng'g, Inc.,* 334 F.3d at 1324.

Although extrinsic evidence can be useful, it is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition is entirely unhelpful to a court. *Id*. Generally, extrinsic evidence is "less reliable than the patent and

its prosecution history in determining how to read claim terms." *Id*.

DISCUSSION

I. The '689 Patent

A. Overview of the Patent

The '689 Patent describes a way to reduce power consumption and conserve the battery life of an electronic device by stopping the device's clock signal. '689 Pat. at 1:59-63. A clock signal is a regularly timed pulse used to synchronize the operations of a microprocessor. PL.'S BR. at 4; DEF'S TECH. TUTORIAL. If a microprocessor stops receiving clock pulses, it will stop executing instructions and enter a "power-down" or "shut-down" mode in which power consumption is reduced. '689 Pat. at 2:25-30. According to the '689 Patent, this method for reducing power consumption was well known in the prior art, but it presented several problems. Software errors or noise could trigger an inadvertent entry into shut down mode, a premature entry into shut down mode, or entry into shut down mode without any means to exit shut down mode. '689 Pat. at 2:22-3:7. The '689 Patent endeavors to solve these problems by requiring that the signal requesting that the device enter shut-down mode conform to a protocol.

Figure 1 shows a clock generator capable of entering shut-down mode:

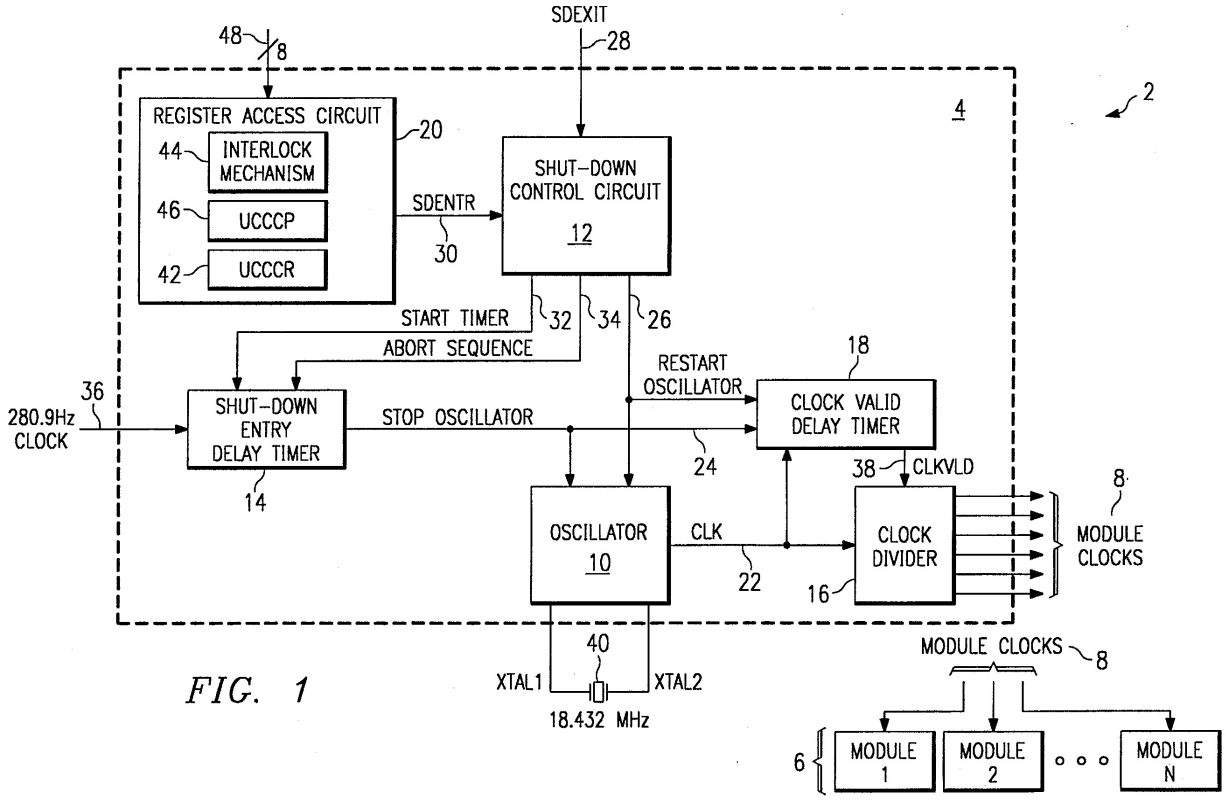
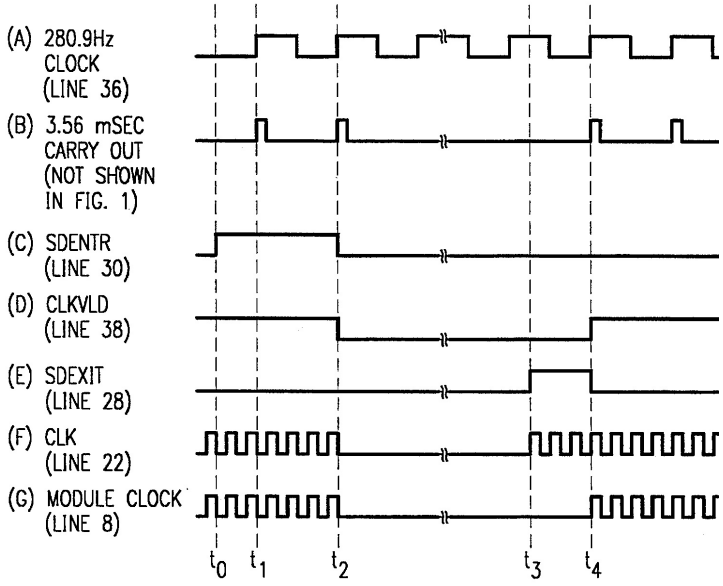


FIG. 1

During normal operation, Oscillator 10 generates regular clock pulses which are ultimately sent to various modules in a device. '689 Pat. at 6:20-22. When the device needs to enter shut down mode, a signal is sent to the clock generator on line 48. '689 Pat. at 7:59-62. Register Access Circuit 20 provides a protection scheme to verify the signal on line 48. '689 Pat. at 7:59-8:16. This protection scheme is a predetermined protocol requirement which avoids inadvertent placement of the clock generator into shut-down mode. Once the signal on line 48 is verified, Register Access Circuit 20 sends a SDENTR signal along line 30 to Shut Down Control Circuit 12. '689 Pat. at 8:14-17. This Circuit sends a START TIMER signal to Shut-Down Entry Delay Timer 14. Timer 14 provides a delay for a "predetermined length of time" to allow one or more of the device modules to enter an idle state. '689 Pat. at 6:59-62. After this delay, a STOP OSCILLATOR signal is sent to Oscillator 10 to stop the clock pulses. The device is now in shut-down mode.

The "predetermined length of time" is calculated by means of a separate clock. This clock, which is external to the clock generator, constantly sends clock pulses to the Shut Down Entry Delay Timer 14 at 280.9 Hz. '689 Pat. at 7:4-10. This clock is significantly slower than the clock pulses of Oscillator 10. Once Timer 14 receives the START TIMER signal, it waits to receive two clock pulses from the external clock, and then sends the STOP OSCILLATOR signal. '689 Pat. at 7:10-16. The timing of this process is shown in Figure 2:

FIG. 2



At time t_0 the SDENTR signal is asserted. '689 Pat. at 8:30-34. At time t_1 Timer 14 receives a first pulse from the external clock. At time t_2, Timer 14 receives the second pulse, and shuts down Oscillator 10. '689Pat. at 8:38-42. At 280.9 Hz, the time between each pulse of the external clock is 3.56ms. Because the SDENTR signal may be asserted at any time, it may take between 3.56ms and 7.12ms for Timer 14 to receive two clock pulses from the external clock. '689 Pat. at 8:38-43.

The following claims are at issue:

5. A method for controlling at least one output clock signal comprising the steps of:
receiving a disable request signal;
stopping said at least one output clock signal after a predetermined length of time after receiving said disable request signal;
receiving an enable request signal; and
starting said at least one output clock signal after receiving said enable request signal,

wherein said step of stopping said at least one output clock signal comprises the steps of verifying that said disable request signal satisfies a predetermined protocol requirement, and processing said disable request signal only if said disable request signal satisfies said predetermined protocol requirement.

[. . .]

8. A method as recited in claim 5 wherein the step of stopping said at least one output clock signal comprises the step of stopping said at least one output clock signal after said predetermined length of time following the most recent assertion of said disable request signal.

B. The Terms in Dispute

The parties present the following terms for construction.

1. "disable request signal"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"disable request signal" Claims 5, 8	a signal to initiate entry into a shut-down mode	a signal that requests the system to stop the output clock signal and that starts the predetermined length of time

Saxon argues that the "disable request signal" corresponds with signal 48 of Figure 1. PL.'S BR. at 5. Defendants argue that the language of claim 5 requires that the "disable request signal" correspond with signal 48 and the SDENTR signal of Figure 1. DEF.'S BR. at 2. They point out that claim 1 describes two separate signals: a "shut-down entry request signal" which corresponds with signal 48, and a "disable activation signal" which corresponds with the SDENTR signal. Claim 5, on the other hand, only recites one signal by name—a "disable request signal." Defendants argue that because this is the only signal identified in claim 5, it must perform both of the functions of the signals identified in claim 1.

Regardless of the merits of Defendants' interpretation of claim 1, Defendants' interpretation of claim 5 is not supported by the plain language of the claim. Claim 5 recites the step of "stopping

said at least one output clock signal . . . after receiving said disable request signal" wherein this signal is processed only if it satisfies a predetermined protocol requirement. In other words, claim 5 recites the steps of (1) receiving a disable request signal, (2) verifying it, and (3) stopping the output clock signal only after the disable request signal has been received and verified and a predetermined length of time has elapsed.[2] There is no requirement that the disable request signal must start the predetermined length of time. In fact, Defendants' interpretation would exclude the figure 1 embodiment, which shows a separate signal initiating the predetermined length of time after signal 48 is verified, from the scope of this claim. *See Globetrotter Software, Inc.*, 362 F.3d at 1381 ("A claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever correct."). Thus, the Court rejects Defendants' proposed construction to the extent that it requires the disable request signal to start the predetermined length of time.

Having resolved the parties' claim scope dispute, the Court must determine how best to construe this term for a lay jury. Defendants argue that Saxon's proposed construction contains two needlessly ambiguous terms: "shut-down mode," and "initiate entry into." Although the term "shut-down mode" does not appear in the language of claim 5, it is adequately described throughout the '689 Patent. The title of this patent is "Clock Generator Capable of Shut-Down Mode and Clock Generation Method." Furthermore, the patent specification consistently describes "shut-down mode" as a power saving mode in which "the clock generator does not generate any clock signals." '689 Pat. at 3:11-15. Therefore, the Court finds that the term "shut-down mode" is not ambiguous. The term

[2] At the hearing, Defendants argued that, because claim 5 requires that the predetermined length of time begin "after" the disable request signal is received, the predetermined length of time must begin immediately after the disable request signal is received. Defendants further argued that this requirement is equivalent to the requirement that the disable requirement signal initiate the predetermined length of time. However, Defendants offer no support for the idea that the word "after" means "immediately after" or "in response to."

"initiate," on the other hand, is more problematic. The patent specification uses this term in a number of different contexts. *See* '689 Pat. at 7:59-64, 8:49-52.

The Court finds that the proper construction of this term is "a signal requesting the system enter into shut-down mode."

2. "predetermined length of time"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"predetermined length of time" Claims 5, 8	an amount of time defined prior to or at the time of receipt of the disable request signal	a definite amount of time fixed prior to receipt of the disable request signal
"stopping said at least one output clock signal after a predetermined length of time after receiving said disable request signal" Claim 5	halting the output clock signal following an amount of time defined prior to or at the time of receipt of the disable request signal	stopping the output clock signal at the expiration of an amount of time that is fixed prior to, and starts from, receipt of the disable request signal

While the parties point out flaws in their respective proposals, according to the parties' technology tutorials, the parties agree on the basic operation of the invention disclosed in the '689 specification. The '689 specification describes a preferred embodiment in which the predetermined length of time varies between 3.56ms and 7.12ms depending on when the SDENTR signal is asserted relative to the external clock. '689 Pat. at 8:30-47. Nonetheless, Defendants appear to argue that claim 5 requires that the predetermined length of time be an exact time, *e.g.* exactly 4ms, rather than a time period, *e.g.* 3.56ms-7.12ms.

Defendants point out that, as originally written, the patentee tried to claim a "predetermined minimum amount of time." Defendants argue that because these claims were abandoned or rejected, the

patentee may not now reclaim subject matter that it abandoned during prosecution. Defendants' argument is misplaced for two reasons. First, by removing the word "minimum" the patentee broadened the scope of its claims; these amendments did not narrow claim scope. For example, a minimum amount of time would be "at least 5ms." A "length of time" may include, "exactly 5ms," "at least 5ms," "between 3ms and 7ms," or "up to 5ms." Second, although the prosecution history cited by Defendants shows that the patentee removed the word "minimum" from the claims, the patentee offered no explanation for why this change was made. This amendment does not clearly and unambiguously disclaim any claim scope, and it certainly does not disclaim the preferred embodiment. *See Omega Eng'g, Inc.*, 334 F.3d at 1323. Accordingly, the Court rejects Defendants proposal to the extent that it limits the predetermined length of time to a predetermined exact time.

The Court finds that Saxon's construction does not clearly encompass the idea that the predetermined length of time refers to a time that may vary within a known time period. The Court finds that the proper construction of the term "predetermined length of time" is "a length of time within a known time period." Because this construction resolves the parties' claim scope dispute, the larger phrase "stopping said at least one output clock signal after a predetermined length of time after receiving said disable request signal" need not be construed. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008); *Fenner Inv. Ltd. v. Microsoft Corp.*, No. 6:07-cv-8, 2008 WL 3981838 at *3 (E.D. Tex. Aug. 22, 2008) (finding that a court need not construe a disputed term as long as it has resolved the claim scope dispute between the parties).

3. "predetermined protocol requirement"

Claim Term	**Plaintiff's Proposal**	**Defendants' Proposal**
"predetermined protocol requirement"	a requirement of a defined protection scheme	Defendants contend that this claim term is more appropriately construed in the context of the larger claim

Claim 5		phrase in which it appears, below.
"verifying that said disable request signal satisfies a predetermined protocol requirement" Claim 5	confirming that said disable request signal meets a requirement of a defined protection scheme	confirming that the received disable request signal satisfies a predetermined series of steps

The primary dispute with regard to these terms is the meaning of the word "protocol." Both parties cite to the definition of "protocol" contained in the same dictionary. *See* IEEE Standard Dictionary of Electrical and Electronic Terms, The Institute of Electrical and Electronics Engineers, Inc., 1984 ("[a] set of conventions or rules that govern the interactions of processes or applications within a computer system"). At the hearing, the Court proposed a construction based on this definition, *i.e.* construing "verifying that said disable request signal satisfies a predetermined protocol requirement" as "confirming that said disable request signal satisfies a known set of rules." *See Markman* Hr'g Tr. at 46:18-20 (June 25, 2009). Saxon agreed to this construction. *Id.* at 47:7-8.Defendants argued that this construction is inconsistent with the patent specification. *Id.* at 47:12-24.

The Court begins its construction by consulting the claim language. *Phillips*, 415 F.3d at 1314. In this case, the plain and ordinary meaning of the term "protocol," as evidenced by the parties' dictionary definitions, is a known set of conventions or rules. Defendants argue that the Court's construction should diverge from this plain and ordinary meaning because the only disclosed example of a predetermined protocol requirement involves a series of sequential steps rather than a set of rules. Defendants cite to the patent specification, which states that "the predetermined protocol requirement may be a predetermined number of writes in a predetermined order to the at least two registers." '689 Pat. at 3:58-60. However, at most, this statement shows that the patent

discloses one embodiment in which the predetermined protocol requirement involves a series of steps. Defendants have not cited any statements of disclaimer, or any other reason to import this limitation into the claim language. *Liebel-Flarsheim Co.*, 358 F.3d at 913; *Brookhill-Wilk 1, LLC*, 334 F.3d 1294, 1301; *see also Phillips*, 415 F.3d at 1312-13.

Saxon's original proposed claim construction is similarly flawed. While the patent explains that the purpose of the predetermined protocol requirement is for protection from inadvertent entry into shut-down mode, '689 Pat. at 8:13-16, Saxon offers no reason to import this purpose into the claim as a limitation. Furthermore, the term "defined protection scheme" would be unnecessarily confusing for a jury.

Therefore, the Court finds that the proper construction for the term "predetermined protocol requirement" is "a known set of rules." Because this construction resolves the parties' claim scope dispute, the larger phrase "verifying that said disable request signal satisfies a predetermined protocol requirement" need not be construed.

II. The '555 Patent

A. Overview of the Patent

The '555 Patent describes a method and system for private wireless communications. Wireless communications generally requires two processes: encryption/decryption, or enciphering/deciphering, and signal processing. For example, during cell phone communications, a cell phone must process the recorded message of the speaker so that it can be sent to a cell tower. Processing may include "encoding, compression, forward error correction and channel equalization of the communication signals." '555 Pat. at 2:4-7. Before the signal is sent, however, it must be encrypted so that only the intended recipient can understand the message. The receiving device must then decrypt the signal and process it.

In the prior art, wireless communications systems required separate circuitry for enciphering/deciphering and signal processing. '555 Pat. at 1:26-37, 2:49-54. This increased the cost of wireless devices and made them less flexible. '555 Pat. at 1:26-55. In contrast, the '555 Patent "utilizes the signal processing circuit of a single chip wireless communications controller not only for processing functions such as communications signal compression, encoding, and radio channel equalization, but also for enciphering and deciphering the processed signals." '555 Pat. at 2:49-53. Saxon has asserted claims 1, 10, 21, 22, 24, 26, 43-46, and 51. Claim 51 is exemplary:

> 51. A communications controller circuit for privately communicating communication signals over a wireless communications network, comprising:
> a signal processing circuit within said communications controller circuit for processing communications signals to form processed communication signals and further for enciphering said processed communication signals; and
> a transceiver associated with said communications controller circuit for transmitting said enciphered and processed communication signals from said communications controller circuit;
> wherein said signal processing circuit comprises circuitry and instructions for enciphering said processed communication signals in said signal processing circuit by programmably selecting an enciphering algorithm.

B. The Terms in Dispute

The parties present the following terms for construction.

1. "signal processing circuit"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51	a circuit, within a communications controller circuit, that executes program instructions to process communications signals and executes program instructions to encipher or decipher such signals	a signal processor that uses the same circuitry to load, store, and execute signal processing instructions and enciphering algorithms

The claims at issue require that enciphering/deciphering and signal processing be performed by a "signal processing circuit." The parties proposed constructions for this term are essentially equivalent

except that Saxon's proposal is broad enough to include general purpose microprocessors and signal processors, but Defendants' proposal requires a "signal processing circuit" to be a signal processor. Saxon argues that Defendant is importing a limitation from the preferred embodiment into the claim language. Defendants argue that the patentee disclaimed broader scope in the specification and the prosecution history.

The claims at issue do not explicitly require that a "signal processing circuit" must be a signal processor. The plain meaning of the word "circuit" implies a broader structure, which may or may not include a signal processor. Thus, the Court will presume that Defendants' proposed construction is improper unless Defendants identify statements of "clear disclaimer" expressly indicating "manifest exclusion or restriction." *Liebel-Flarsheim Co.*, 358 F.3d at 913; *Brookhill-Wilk 1, LLC*, 334 F.3d 1294, 1301; *see also Phillips*, 415 F.3d at 1312-13.

Defendants argue that the only embodiment disclosed in the specification is one in which enciphering/deciphering and signal processing are performed by a single digital signal processor ("DSP"), rather than different portions of circuitry within a circuit. '555 Pat. at 4:39-47, 6:52-55. Defendants further argue that the patentee disclaimed broader embodiments when it told the PTO that "[e]ach of Claims 1, 21 and 43 require signal processors having an integrated ability to perform enciphering or deciphering functions." '555 Pat. Amendment at 30 (July 17, 1996). The patentee made this statement to distinguish a prior art reference which incorporated separate devices to perform the enciphering/deciphering and signal processing functions. *Id.* However, in the same paragraph, the patentee also stated that the prior art reference was distinguishable because the claimed invention "implements encryption/decryption as an additional task performed by the signal processing circuit." *Id.*

While the Court recognizes Defendants' concern that the patentee should not be able to acquire claim scope over devices present in the prior art, Defendants have not shown that the patentee has

disclaimed claim scope. *Omega Eng'g, Inc.,* 334 F.3d at 1324. While Defendants are correct that the only embodiment discussed in detail uses a DSP to perform enciphering/deciphering and signal processing, Defendants have not shown that the limitation of this embodiment should be imported into the claims. *See Comark Commc'ns, Inc.*, 156 F.3d at 1187. In fact, the patent specification contemplates a variety of embodiments. '555 Pat. at 10:52-59 (stating that "[t]he present invention makes possible digital signature authentication and message encryption using either a single DSP or a single microprocessor, or using both a DSP and a microprocessor"). Similarly, Defendants have not presented a valid prosecution disclaimer argument. At best, Defendants have cited to an ambiguous passage in the prosecution history. *Cf. Omega Eng'g, Inc.,* 334 F.3d at 1323.

Saxon's proposed construction is consistent with the specification's use of the term "signal processing circuit." '555 Pat. at 10:23-28. However, the phrase "within a communications controller circuit" is superfluous since this limitation is already present in the claims. The Court finds that the proper construction for this term is "a circuit that executes program instructions to process communications signals and executes program instructions to encipher or decipher such signals."

2. "processing (the) . . . communication signals"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"processing (the). . . communication(s) signals" Claims 1, 10, 21, 43, 51	performing a signal processing operation on (the) communication(s) signals	modifying the data to be transmitted prior to enciphering or after deciphering

Saxon argues that Defendants' proposal is confusing because the word "modifying" is not present in the claim language. Defendant argues that every example of "processing" contained in the '555 Patent necessarily involves some modification of data. *See, e.g.,* '555 Pat. at 2:4-6 ("Processing may include encoding, compression, forward error correction, and channel equalization of the communication

signals."). In its reply brief, Saxon explained that, to the extent that the word "modifying" covers the examples of processing described in the patent, the parties apparently agree on the scope of this term. The parties did not address this term at the hearing.

Based on the arguments before the Court, the Court is unable to discern any claim scope dispute with regard to this term. Defendants do not cite to any intrinsic evidence that uses the term "modifying," or explained how their proposal differs from Saxon's proposal, which more closely follows the language of the claims at issue. Accordingly, the Court adopts Saxon's proposed construction.

3. "enciphering (the) (said) processed communication signals"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"enciphering (the) (said) processed communication signals" Claims 1, 10, 21, 26, 43, 45, 51	applying an enciphering algorithm to encrypt (the) (said) processed communication signals	applying an enciphering algorithm to the processed communication signals to make the processed communication signals private

The parties' proposals are essentially the same except that Defendants' proposal requires that the enciphering algorithm make the processed communication signals private. This additional limitation is not present in the claim language, and, although the specification describes this feature as a benefit of the invention, the Court sees no reason to insert it as a claim limitation. *See Comark Commc'ns, Inc.*, 156 F.3d at 1187. Accordingly, the Court adopts Saxon's proposed construction.

4. "programmably selecting an enciphering algorithm"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"programmably selecting an enciphering algorithm" Claims 10, 51	executing in a signal processing circuit a set of program instructions to select one of a plurality of enciphering algorithms	executing a set of program instructions to select one from among a plurality of enciphering algorithms

The parties proposals are essentially the same, except that Saxon's proposal contains the additional limitation that the selection of an enciphering algorithm must occur in the signal processing circuit. Defendants argue that this limitation excludes embodiments disclosed in the specification. *See* '555 Pat. at 4:43-44, 4:57-59, Fig. 3.

While the Court is mindful of the fact that a construction which would result in excluding the preferred, and only, embodiment "is rarely, if ever, correct," *Globetrotter Software, Inc.*, 362 F.3d at 1381, the Court may not redraft claim language. *See Lucent Techs., Inc. v. Gateway, Inc.*, 525 F.3d 1200, 1215 (Fed. Cir. 2008). In this case, Claim 10 states: "enciphering said processed communication signals *in said first signal processing circuit* by programmably selecting an enciphering algorithm" (emphasis added). Claim 51 states: "said signal processing circuit comprises circuitry and instructions for enciphering said processed communication signals *in said signal processing circuit* by programmably selecting an enciphering algorithm" (emphasis added). These statements require that enciphering occur in a signal processing circuit, and that the enciphering be accomplished by programmably selecting an enciphering algorithm. Thus, these statements require the selection of the enciphering algorithm to occur in the signal processing circuit.

Even if Defendants are correct that Saxon's proposal excludes an embodiment disclosed in the specification, the Court cannot simply disregard this claim language. Accordingly, the Court adopts Saxon's proposed construction.

5. "enciphering/deciphering algorithm"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"enciphering algorithm" Claims 10, 26, 45, 51	a prescribed set of well-defined rules or processes for the solution of a problem in a finite number of steps	a series of steps for encrypting signals

"deciphering algorithm" Claim 46	a prescribed set of well-defined rules or processes for the solution of a problem in a finite number of steps	a series of steps for decrypting signals

The primary dispute with regard to this term is the meaning of the word "algorithm." At the hearing, Saxon proposed that the construction of this word be based on the dictionary definitions cited by Defendants. *See Markman* Hr'g Tr. at 106:4-15; *Newton's Telecom Dictionary* (10th ed. 1996)) (defining algorithm as "[a] prescribed finite set of well defined rules or processes for the solution of a problem in a finite number of steps."); *IEEE Standard Dictionary of Electrical and Electronic Terms* (1988) (defining algorithm as "[a] prescribed set of well-defined rules or processes for the solution of a problem in a finite number of steps"). Defendants argued that their proposal would be easier for a jury to understand.[3]

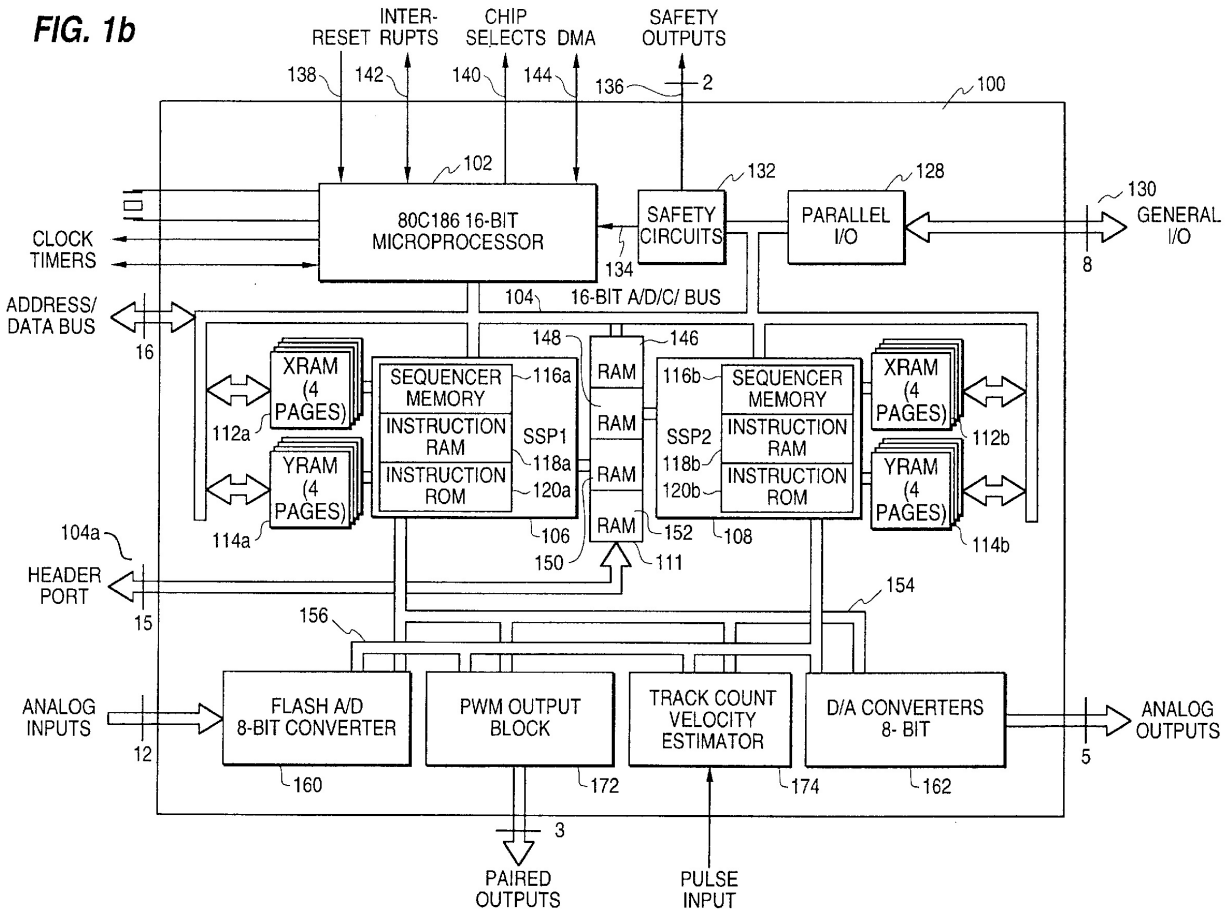
The Court finds that the dictionary definition offered by Defendants may be easily understood by a jury. However, the Court's construction need not include the general purpose of an algorithm, *e.g.*, "for the solution of a problem in a finite number of steps," because the claim terms specify specific purposes. Accordingly, the Court construes "enciphering algorithm" as "a prescribed set of well defined rules or processes for encrypting signals." The Court construes "deciphering algorithm as "a prescribed set of well defined rules or processes for decrypting signals."

[3] The only evidence cited by Defendants to support their proposals are the dictionary definitions cited above. The Court finds these definitions to be inconsistent with Defendants' proposals.

III. The '394 Patent

A. Overview of the Patent

The '394 Patent discloses a microprocessor system with a master processor and multiple slave processors. The Patent overcomes, *inter alia*, the risk of overwriting data that is saved to one location by multiple processors. Pl.'s Br. at 22. One embodiment is shown in Figure 1b:



The Figure 1b embodiment includes a master processor 102 and slave signal processors 106 and 108. These processors are connected to Random Access Memory ("RAM") 111 by a bus. RAM 111 is divided into four blocks. Each processor can write data to only one separate block of RAM 111. '394 Pat. at 5:17-22. Each processor can read from any block of RAM 111. '394 Pat. at 5:24-26. "[T]o exchange information between processors, for example, between streamlined signal processor

106 and microprocessor 102, the processor with information writes its data to its own block of RAM . . . and signals the recipient (microprocessor 102) to read the sender's RAM block." '394 Pat. at 5:26-32.

B. The Terms in Dispute

The parties present the following terms for construction.

1. "signal processor"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"signal processor" Claim 11	processor for executing instructions to perform programmed tasks	a programmable device that interprets and executes instructions for performing signal processing

Defendants argue that a signal processor is a processor specifically tailored to perform signal processing operations. Saxon argues that this term refers to a general purpose microprocessor, which need not be specifically designed to perform signal processing.[4] Contrary to Saxon's argument, the '394 Patent reinforces the idea that there is a generally recognized distinction between signal processors and general purpose microprocessors.

The '394 Patent specification states: "The above and other objectives of the invention are accomplished by a system which includes a general purpose microprocessor and one or more streamlined signal processors to which critical functions can be dedicated." '394 Pat. at 2:5-8. This statement strongly implies that a "signal processor" is not simply a synonym for a "general purpose microprocessor." The Court finds that Saxon's proposal would read the word "signal" out of the claim term at issue. Therefore, the Court adopts Defendants' proposed construction.

[4] This position is arguably inconsistent with Saxon's proposed construction for the term "signal processing circuit" discussed above, which Saxon supported by arguing that the term was broad enough to cover "both a DSP and a general microprocessor." PL.'S REPLY at 6.

2. "master processor"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"master processor" Claim 1	general purpose processor not under control of a signal processor	a general purpose microprocessor, not under the control of a signal processor, that controls the apparatus

The parties agree that a master processor is not under the control of a signal processor, but Defendants propose that a master processor must also control the apparatus. Defendants argue that Saxon's proposal disregards the word "master" in the claim term. Saxon argues that the term "master" refers only to the fact that the processor is not under the control of a signal processor.

Defendant's proposed additional limitation is not present in the claim language. While, the specification does describe an embodiment wherein a master processor controls the apparatus, '394 Pat. at 2:15-16, the Court sees no reason to import this limitation into the claim at issue. The Court's conclusion is bolstered by the prosecution history, in which the patentee explained that a "master" processor "does not allow a slave processor to take over control of the master processor at any time." '394 Pat. Amendment at 5 (Aug. 26, 1997). This explanation is consistent with Saxon's proposal and makes no mention of Defendant's proposed additional limitation.

The Court finds that Saxon's proposal adequately explains the plain and ordinary meaning of "master processor," and thus it does not read the word "master" out of the term. The Court adopts Saxon's proposed construction.

3. "each signal processor having write access . . ."

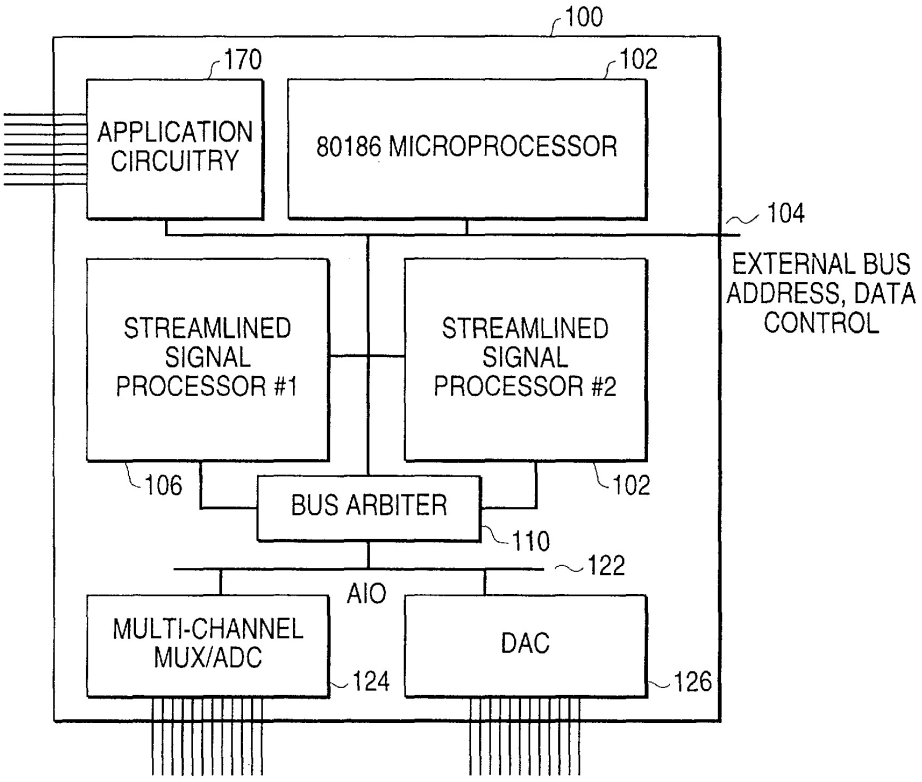
Claim Term	Plaintiff's Proposal	Defendants' Proposal
"each signal processor having write access at any time to only a particular one of said memories and read access at any time to	each of said plurality of signal processors being able to write to only a particular memory location, and said each of said plurality of signal processors being able to read from said particular memory location as	each signal processor can always: (1) write without delay to only its exclusive memory; and (2) read without delay from any of the memories

any of said memories" Claim 11	well as other respective particular memory locations	

The parties dispute the meaning of the language "at any time." Defendants argue that this limitation requires that each signal processor have read access and write access "without latency" or, in other words, "without delay." They further argue that Saxon reads the "at any time" language out of the term. Saxon argues that the "at any time" limitation refers to asynchronous operation of multiple processors, *i.e.* the idea that the processors need not all write at the same time or all read at the same time.

In addition to the Figure 1b embodiment discussed above, the patent also discloses an embodiment containing multiple processors, in which each processor does not have its own designated memory. '394 Pat. at 5:5-6. This embodiment is shown in Figure 1a:

FIG. 1a



The Figure 1a embodiment contains a bus arbiter 110 which controls access to the bus. If, for example, both signal processors 106 and 102 need to access system memory at the same time a collision will occur. '394 Pat. at 4:1-3. During a colliding access request, Bus Arbiter 110 assigns priority to one of the processors and only that processor will be able to access system memory. '394 Pat. at 4:8-13. In the meantime, the other processor remains stalled until it has access to the bus. '394 Pat. at 4:13-15. One of the benefits of the Figure 1b embodiment is that it avoids this stalling, *i.e.* it allows each processor to access memory "without latency." '394 Pat. at 5:18-26.

Defendants argue that the "at any time" limitation of this term refers to the Figure 1b embodiment and the fact that this embodiment allows write access and read access for each processor without latency. Saxon argues that this limitation refers to a more fundamental distinction over the prior art. Specifically, Saxon argues that the "at any time" limitation merely requires that the multiple processors be able to operate asynchronously. Saxon bases its argument on the prosecution history.

During prosecution, the patentee distinguished a prior art reference that also contained multiple processors ("Cutts"). *See* '394 Pat. Amendment at 1 (June 6, 1995). The patentee argued that Cutts disclosed a system in which each processor may have access to designated memories, but all of the processors operate on identical instruction streams. Thus, they would all read at the same time or write at the same time. '394 Pat. Amendment at 2. The patentee described Cutts as requiring synchronous operation. '394 Pat. Amendment at 3. In contrast, the patentee explained that "in the present invention, a processor's ability to write to any memory location in its area at any time allows the processors to execute entirely different and unrelated streams of instructions and to operate asynchronously of each other." '394 Pat. Amendment at 3. Furthermore, "[t]his ability for a processor to write to any of its memory locations at any time eliminates data write latency." '394

Pat. Amendment at 2-3. Based on this prosecution history, Saxon argues that the "at any time" limitation distinguishes systems that require synchronous operation, not systems that have data write latency.

Viewed in isolation, the phrase "at any time" could refer to asynchronous operation, but in the context of the entire claim, Saxon's position cannot stand. *Phillips*, 415 F.3d at 1314("the context in which a term is used in the asserted claim can be highly instructive"). Claim 11 requires that each signal processor have write access or read access at any time. The Figure 1a embodiment does not satisfy this limitation because each processor has read or write access only when no other processor has access. Cutts does not satisfy this limitation because each processor has read or write access only when every processor has read or write access. Thus, Saxon's argument that the "at any time" limitation was only meant to distinguish Cutts does not account for the fact that this limitation excludes systems with data read/write latency. Furthermore, while Saxon is correct that Claim 11 distinguishes systems that require synchronous operation, it distinguishes those systems by requiring that "at least one of said signal processors in said plurality operates independently of other signal processors."

To summarize, the parties have presented two different contexts in which data read/write latency may arise: (1) when bus access is limited, *e.g.* the Figure 1a embodiment, or (2) when multiple processors operate on identical instruction streams, *e.g.* Cutts. The Court finds that the "at any time" limitation excludes both embodiments. As explained above, neither the Figure 1a embodiment nor Cutts allows read and write access for each processor "without latency." Because Saxon's proposal does not account for the "at any time" limitation, it must be rejected. Defendants proposal, on the other hand,

appropriately describes this limitation as "without delay."[5] Accordingly, the Court adopts Defendants' proposed construction.

4. "at least one of said signal processors . . ."

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"at least one of said signal processors in said plurality operates independently of other signal processors" Claim 11	one (1) or more of the signal processors of said plurality of signal processors executes instructions autonomously from another one of said signal processors	at least one signal processor can operate without being interrupted by any of the two or more other signal processors

The parties dispute whether this term requires the presence of two or more signal processors or three or more signal processors. Saxon argues that because the term uses the word "plurality," the claim only requires two or more signal processors. *See, e.g., Dayco Prods., Inc. v. Total Containment, Inc.*, 258 F.3d 1317, 1327-28 (Fed. Cir. 2001) ("'plurality,' when used in a claim refers to two or more items, absent some indication to the contrary"). Saxon argues that "[t]he actual claim language requires two or more signal processors, with one of the two or more signal processors operating independently of one or more signal processors." Defendants argue that the plain language of the term requires three or more signal processors.

Saxon's argument focuses on the word "plurality," and ignores the other limitations in the claim. While the term does recite a "plurality" of signal processors, it also states that at least one signal processor must operate independently of other signal processors. This is an undeniable

[5] Saxon also argues that this "without delay" limitation is inappropriate because it is not physically possible. Saxon is correct that no processor can read or write to memory instantaneously. *See, e.g., Paragon Solutions, LLC v. Timex Corp.*, No. 2008-1516, 2009 WL 1424443 at * 11 (Fed. Cir. May 22, 2009) (finding that "'real time' cannot mean instantaneous"). Nonetheless, at the hearing, Defendants explained that they will not argue that this limitation requires an accused product to defy the laws of physics. *Markman* Hr'g Tr. at 117:18-118:6. Thus, Saxon's concern is unfounded.

"indication to the contrary," *id.*, that, at a minimum, the claim requires one signal processor to operate independently of two signal processors. Thus, the "plurality" referred to in the term must consist of three or more signal processors. The Court adopts Defendants' proposed construction.

5. "respective indication signal"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"respective indication signal" Claim 11	a respective signal to said master processor so as to indicate to said master processor	a signal generated by a signal processor that instructs the master processor to read that signal processor's exclusive memory
"wherein said signal processors provide a respective indication signal to said master processor so as to notify said master processor that newly-written-in data can be obtained" Claim 11	wherein said signal processors provide a respective signal to said master processor so as to indicate to said master processor that a corresponding signal processor has written readable data	Defendants contend that the construction of this phrase is unnecessary in light of Defendants' proposed construction for the claim term above.

Defendants' proposal inserts a limitation not present in the claim language, *i.e.* that the signal instruct the master processor to read from memory. For support, Defendants cite to the specification which states: "the processor . . . signals the recipient (microprocessor 102) to read from the sender's RAM block." '394 Pat. at 6:58-62. This passage appears in a general description of how the processors of the invention share information. Even if it could be interpreted as disclosing an embodiment in which a signal processor instructs the master processor, Defendants offer no reason for the Court to import this limitation into the claim language. Furthermore, Defendants' proposal is inconsistent with the Court's construction of "master processor." As explained above, and as agreed by the parties, a master processor is not under the control of a signal processor.

The Court finds that Saxon's constructions are also deficient because they merely restate the claim language and replace the word "notify" with the word "indicate." The Court finds that these terms will be easily understood by a jury, and that no construction is necessary for either of these terms.

6. "respective portions of a same memory"

Claim Term	Plaintiff's Proposal	Defendants' Proposal
"respective portions of a same memory" Claim 12	allocated corresponding memory locations within a memory unit	Defendants contend that this claim term is more appropriately construed in the context of the larger claim phrase in which it appears, below
"said plurality of memories comprise respective portions of a same memory" Claim 12	said plurality of memories comprise allocated corresponding memory locations of a single memory device	the plurality of memories are respective blocks of a single memory device

Although the parties have not expressed agreement for this term, the Court is unable to discern a substantive difference between the parties' proposals. Because Saxon's proposal more closely follows the actual claim language, the Court adopts Saxon's proposed construction for the term "said plurality of memories comprise respective portions of a same memory." The Court finds that no separate construction is necessary for the term "respective portions of a same memory."

IV. Agreed Term

Prior to the hearing, the parties agreed that the term "communications controller circuit," which appears in the '555 Patent should be construed as "a single chip wireless communications controller."

CONCLUSION

For the foregoing reasons, the Court interprets the claim language in this case in the manner set forth above. For ease of reference, the Court's claim interpretations are set forth in a table attached to this opinion as Appendix A.

So ORDERED and SIGNED this 30th day of July, 2009.

JOHN D. LOVE
UNITED STATES MAGISTRATE JUDGE

APPENDIX A

U.S. Pat No. 5,502,689

'689 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
5. A method for controlling at least one output clock signal comprising the steps of: receiving a disable request signal;	"disable request signal" Claims 5, 8	a signal to initiate entry into a shut-down mode <u>Intrinsic Evidence:</u> '689 patent: Col. 7:58-62; Fig. 1 <u>Extrinsic Evidence:</u> See "signal" in The New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Edition, IEEE Std 100-1992, Copyright 1993, p. 1218	a signal that requests the system to stop the output clock signal and that starts the predetermined length of time <u>Intrinsic Evidence:</u> '689 patent: Abstract; Col. 4, ll. 63-67; Col. 6, ll. 20-22, 29-35, 40-47, 57-59; Col. 7, l. 59 – Col. 8, l. 16; Col. 8, ll. 10-13, 26-48; Col. 8, l. 66 - Col. 9, l. 10; Col. 9, ll. 1-3, 14-19, 48-53; Fig. 1; Claim 8.	A signal requesting the system enter into shut down mode
stopping said at least one output clock signal after a predetermined length of time after receiving said disable request signal;	"predetermined length of time" Claims 5, 8	an amount of time defined prior to or at the time of receipt of the disable request signal <u>Intrinsic Evidence:</u> '689 patent: Col. 3:30-33; Col. 3:36-38; Col. 4:52-53; Col. 6:57-62; Col. 7:4-7; Col. 7:16-21; Col. 8:42-44	a definite amount of time fixed prior to receipt of the disable request signal <u>Intrinsic Evidence:</u> '689 patent: Abstract; Col. 4, ll. 63-67; Col. 7, ll. 4-27; Col. 8, ll. 26-48; Col. 9, ll. 48-53. <u>Intrinsic Evidence from the '689 File History:</u>	A length of time within a known time period

'689 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
			'689 Patent File History, Original Application, at 30; Office Action (Dec. 27, 1994), at 2; Amendment Under 37 C.F.R. § 1.111 (June 8, 1995), at 2. Extrinsic Evidence: "predetermine: To determine, decide, or establish ahead of time." Webster's II New Riverside University Dictionary, Houghton Mifflin Co., 1988. "predetermine: determine beforehand." Webster's Ninth New Collegiate Dictionary, Merriam-Webster, Inc., 1986.	
stopping said at least one output clock signal after a predetermined length of time after receiving said disable request signal;	"stopping said at least one output clock signal after a predetermined length of time after receiving said disable request signal" Claim 5	halting the output clock signal following an amount of time defined prior to or at the time of receipt of the disable request signal Intrinsic Evidence: '689 patent: Col. 3:30-33; Col. 3:36-38; Col. 4:52-53; Col. 6:57-62; Col. 7:4-7; Col. 7:16-21; Col. 8:42-44; Col. 9:	stopping the output clock signal at the expiration of an amount of time that is fixed prior to, and starts from, receipt of the disable request signal Intrinsic Evidence: '689 patent: Abstract; Col. 2, ll. 25-30; Col. 2, ll. 52-56; Col. 3, ll. 34-39; Col. 4, ll. 63-67; Col. 6,	No construction necessary

'689 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
		3-8; Col. 8:45-46; Fig. 2; Fig. 3 Extrinsic Evidence: See "stopping (5.)" in The American Heritage College Dictionary, 1993, Houghton Mifflin, pp. 1338-1339 See "clock" in The New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Edition, IEEE Std 100-1992, Copyright 1993, p. 196 See "clock" in Newton's Telecom Dictionary, 5th Edition, 1992, Flatiron Publishing, Inc., p. 197 See "after" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 24 See "receiving" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 1139	ll. 11-14; Col. 6, ll. 29-36; Col. 6, ll. 40-47; Col. 6, ll. 57-62; Col. 8, ll. 26-46; Col. 7, ll. 4-27; Figure 2. Intrinsic Evidence: Abstract; Col. 4, ll. 63-67; Col. 7, ll. 4-27; Col. 8, ll. 26-48; Col. 9, ll. 48-53. Intrinsic Evidence from the '689 File History: '689 Patent File History, Original Application, at 30; Office Action (Dec. 27, 1994), at 2; Amendment Under 37 C.F.R. § 1.111 (June 8, 1995), at 2. Extrinsic Evidence: "predetermine: To determine, decide, or establish ahead of time." Webster's II New Riverside University Dictionary, Houghton Mifflin Co., 1988. "predetermine: determine beforehand." Webster's Ninth New Collegiate Dictionary, Merriam-Webster,	

'689 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
			Inc., 1986, p. 926.	
receiving an enable request signal; starting said at least one output clock signal after receiving said enable request signal; wherein said step of stopping said at least one output clock signal comprises the steps of verifying that said disable request signal satisfies a predetermined protocol requirement, and processing said disable request signal only if said disable request signal satisfies said predetermined protocol requirement.	"predetermined protocol requirement" Claim 5	a requirement of a defined protection scheme Intrinsic Evidence: '689 patent: Col. 3:47-51; Col. 3:58-60; Col. 4:50-53; Col. 7:65-67; Col. 8:13-15; Fig. 1 Extrinsic Evidence: See "protocol" in The New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Edition, IEEE Std 100-1992, Copyright 1993, p. 1022 See "requirement" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 1160	Defendants contend that this claim term is more appropriately construed in the context of the larger claim phrase in which it appears, below.	A known set of rules
wherein said step of stopping said at least one output clock signal comprises the steps of verifying that said disable request signal satisfies a	"verifying that said disable request signal satisfies a predetermined protocol requirement"	confirming that said disable request signal meets a requirement of a defined protection scheme Intrinsic Evidence: '689 patent: Col. 7:58-62;	confirming that the received disable request signal satisfies a predetermined series of steps Intrinsic Evidence: '689 patent: Col. 3, ll. 46-60; Col. 7, l. 58 - Col. 8, l. 16; Col.	No construction necessary

'689 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
predetermined protocol requirement, and processing said disable request signal only if said disable request signal satisfies said predetermined protocol requirement.	Claim 5	Fig. 1; Col. 3:47-51; Col. 3:58-60; Col. 4:50-53; Col. 7:65-67; Col. 8:13-15 Extrinsic Evidence: See "verification" in The New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Edition, IEEE Std 100-1992, Copyright 1993, p. 1455. See "verify" in the Microsoft Press Computer Dictionary, 1991, Microsoft Press, p. 360. See "verifying (2.)" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 1499. See "satisfies (5.)" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 1213	8, ll. 8-10, 13-16. Extrinsic Evidence: "Protocol - (1) (data communication) - A formal set of conventions governing the format and relative timing of messages exchanged between two communications terminals. (2) (software) - (A) A set of conventions or rules that govern the interactions of processes or applications within a computer system or network. (B) A set of rules that govern the operation of functional units to achieve communication." IEEE Standard Dictionary of Electrical and Electronic Terms, The Institute of Electrical and Electronics Engineers, Inc., 1984. "predetermine: To determine, decide, or establish ahead of time." Webster's II New Riverside University Dictionary, Houghton Mifflin Co., 1988. "predetermine: determine	

'689 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
			beforehand." Webster's Ninth New Collegiate Dictionary, Merriam-Webster, Inc., 1986.	
8. A method as recited in claim 5 wherein the step of stopping said at least one output clock signal comprises the step of stopping said at least one output clock signal after said predetermined length of time following the most recent assertion of said disable request signal.	"disable request signal" "predetermined length of time" Claims 5, 8	See Claim 5, above.	See Claim 5, above.	

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
1. A method for privately communicating over a wireless communications network, comprising the steps of: processing the communication signals in a first signal processing circuit within a first communications controller circuit at a first location to produce processed communication signals;	"communications controller circuit" Claims 1, 10, 21, 43, 51	[AGREED]	[AGREED]	a single chip wireless communications controller
processing the communication signals in a first signal processing circuit within a first communications controller circuit at a first location to produce	"signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51	a circuit, within a communications controller circuit, that executes program instructions to process communications signals and executes program instructions to encipher or decipher such	a signal processor that uses the same circuitry to load, store, and execute signal processing instructions and enciphering algorithms Intrinsic Evidence from the '555	A circuit that executes program instructions to process communications signals and executes program instructions to encipher or decipher such signals

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
processed communication signals;		signals Intrinsic Evidence: '555 patent: Col. 2:49-54; Col. 4:29-35; Col. 6:1-4; Col. 10:23-32; Col. 10:58; Fig. 2; Fig. 3; Amendment 7/17/1996, p. 30.	File History: '555 Patent File History, "Amendment" (July 17, 1996) at 30-31, *et al.* '555 Patent File History, "Amendment" (July 17, 1996) at 31, *et al.* Intrinsic Evidence from the '555 Specification: '555 patent: Col. 2, ll. 49-54; Col. 4, ll. 39-47; Col. 5, ll. 3-7; Col. 5, l. 66 - Col. 6, ll. 2, 52-55; Col. 6, ll. 3-17; Col. 6, ll. 52-55; Col. 11, ll. 6-13; Claim 1.	
processing the communication signals in a first signal processing circuit within a first communications controller circuit at a first location to produce processed communication signals;	"processing (the) …. communication (s) signals" Claims 1, 10, 21, 43, 51	performing a signal processing operation on (the) communication(s) signals Intrinsic Evidence: '555 patent: Col. 2:4-6; Col. 9:25-44; Col. 10:23-32.	modifying the data to be transmitted prior to enciphering or after deciphering Intrinsic Evidence: '555 patent: Col. 1, l. 67 - Col. 2, l. 4; Col. 2, ll. 4-12, 23-27, 49-54; Col. 5, ll. 3-7; Col. 11, ll. 6-13, 26-28. Extrinsic Evidence Newton's Telecom Dictionary, 10th Edition, 1996, Flatiron Publishing,	Performing a signal processing operation on (the) communication(s) signals

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
			Inc., p. 436, defining "encoding" as "[t]he process of converting data into code or analog voice into a digital signal." Alan Freedman, The Computer Glossary (6th ed. 1993), p. 240, defining "forward error correction" as "Before transmission, the data is processed through an algorithm that adds extra bits for error correction."	
enciphering the processed communication signals in the first signal processing circuit at said first location to produce enciphered and processed communication signals; transmitting the enciphered and processed communication signals between a first location and a second location using the first communications	"enciphering (the) (said) processed communication signals" Claims 1, 10, 21, 26, 43, 45, 51	applying an enciphering algorithm to encrypt (the) (said) processed communication signals <u>Intrinsic Evidence:</u> '555 patent: Col. 1:17-19; Col. 3:6-11; Col. 4:18-35; Col. 8:23-25; Col. 8:52-56; Col. 9:45-58 <u>Extrinsic Evidence:</u> See "encipher" and "encryption" in the Microsoft Press Computer Dictionary, Third Edition,	applying an enciphering algorithm to the processed communication signals to make the processed communication signals private <u>Intrinsic Evidence:</u> '555 patent: Col. 7, ll. 1-4; Col. 8, l. 67-Col. 9, l. 13; title.	Applying an enciphering algorithm to encrypt (the) (said) processed communication signals

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
controller circuit at said first location; receiving the enciphered and processed communication signals at the second location using a second communications controller circuit; deciphering the enciphered and processed communication signals in a second signal processing circuit within the second communications controller circuit at said second location; and processing the deciphered and processed communication signals in the second signal processing circuit to produce communications		1997, Microsoft Press, p. 175; See "encryption" in Newton's Telecom Dictionary, 10th Edition, 1996, Flatiron Publishing, Inc., pp. 436-437		

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
signals at the second location.				
10. A method for privately communicating over a wireless communications network, comprising the steps of: processing the communication signals in a first signal processing circuit within a first communications controller circuit at a first location to produce processed communication signals; enciphering the processed communication signals in the first signal processing circuit at said first location to	"communications controller circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51 "signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51 "processing (the) … communication(s) signals" Claims 1, 10, 21, 43, 51	Please see above, Claim 1	Please see above, Claim 1	

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
produce enciphered and processed communication signals; transmitting the enciphered and processed communication signals between a first location and a second location using the first communications controller circuit at said first location; receiving the enciphered and processed communication signals at the second location using a second communications controller circuit; deciphering the enciphered and processed communication signals	"enciphering (the) (said) processed communication signals" Claims 1, 10, 21, 26, 43, 45, 51			

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
in a second signal processing circuit within the second communications controller circuit at said second location; and processing the deciphered and processed communication signals in the second signal processing circuit to produce communications signals at the second location;				
wherein said enciphering step further comprises the step of enciphering said processed communication signals in said first signal processing circuit by programmably selecting an	"programmably selecting an enciphering algorithm" Claims 10, 51	executing in a signal processing circuit a set of program instructions to select one of a plurality of enciphering algorithms <u>Intrinsic Evidence:</u> '555 patent: Col. 4:57-64; Col. 7: 4-7; Col. 7:37-39; Col. 10:11-17; Fig. 6	executing a set of program instructions to select one from among a plurality of enciphering algorithms <u>Intrinsic Evidence:</u> '555 patent: Col. 2, ll. 54-58; Col. 3, ll. 2-5, 6-8; Col. 4, ll. 43-44, 57-66; Col. 6, ll. 32-37; Col. 12, ll. 53-61; Col. 20, ll. 21-23; Fig. 3; Fig.	Executing in a signal processing circuit a set of program instructions to select one of a plurality of enciphering algorithms

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
enciphering algorithm.		Extrinsic Evidence: See "programmable" in The New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Edition, IEEE Std 100-1992, p. 1014	6.	
wherein said enciphering step further comprises the step of enciphering said processed communication signals in said first signal processing circuit by programmably selecting an enciphering algorithm.	"enciphering algorithm" Claims 10, 26, 45, 51	a prescribed set of well-defined rules or processes for the solution of a problem in a finite number of steps Intrinsic Evidence: '555 patent: C. 1, L. 28-30; C. 7, L. 45-61; C. 8, L. 53-54; C. 10, L. 56-63; Fig. 6 Extrinsic Evidence: See, e.g., "encryption" in Newton's Telecom Dictionary, 10th Edition, 1996, Flatiron Publishing, Inc., pp. 436-437; See, e.g., "encryption" in the Microsoft Press Computer Dictionary, Third Edition, 1997, Microsoft Press, p. 175	a series of steps for encrypting signals Extrinsic Evidence: IEEE Standard Dictionary of Electrical and Electronic Terms, The Institute of Electrical and Electronics Engineers, Inc., 1988, p. 29, defining "Algorithm" as "(1) (general) - A prescribed set of well-defined rules or processes for the solution of a problem in a finite number of steps. (2) (software) - (1) a finite set of well-defined rules for the solution of a problem in a finite number of steps; (2) a finite set of well-defined rules which gives a sequence of operations for performing a specific task."	A prescribed set of well defined rules or processes for encrypting signals

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
		See, e.g., "algorithm" in Newton's Telecom Dictionary, 10th Edition, 1996, Flatiron Publishing, Inc., p. 66	Newton's Telecom Dictionary, 10th Edition, 1996, Flatiron Publishing, Inc., p. 66, defining "algorithm" as "[a] prescribed finite set of well defined rules or processes for the solution of a problem in a finite number of steps." Newton's Telecom Dictionary, 18th Edition, 2002, CMP Books. p. 102, defining "block cipher" as "A digital encryption method which ciphers long messages by segmenting them into blocks of fixed length, prior to encryption. Each block, which typically is 64 bits in length, is encrypted individually. The blocks may be sent as individual units, or they may be linked in a method knows [sic] as Cipher-Block-Chaining."	

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
21. A system for privately communicating communications signals over a wireless communications network, comprising: a first communications controller at a first location; a first signal processing circuit within said first communications controller circuit at the first location for processing communications signals to form processed communication signals and further for enciphering said processed communication signals; a first transceiver associated at said first location with said first communications	"communications controller circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51 "signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51 "processing (the) … communication(s) signals" Claims 1, 10, 21, 43, 51 "enciphering (the) (said)	Please see above, Claim 1	Please see above, Claim 1	

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
controller for transmitting said enciphered and processed communication signals between said first location and a second location; a second communications controller circuit at the second location for controlling communications at said second location; a second transceiver associated at the second location with said second communications circuit for receiving said enciphered and processed communication signals from said first transceiver; a second signal processing circuit within said second communications controller circuit at the second location for	processed communication signals" Claims 1, 10, 21, 26, 43, 45, 51			

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
deciphering said received enciphered and processed communication signals, said second signal processing circuit further for processing said deciphered and processed communication signals.				
22. The system of claim 21, wherein said first signal processing circuit comprises a first digital signal processing circuit.	"signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51	Please see above, Claim 1	Please see above, Claim 1	
24. The system of claim 21, wherein said second signal processing circuit comprises a second digital signal processing circuit.	"signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51	Please see above, Claim 1	Please see above, Claim 1	

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
26. The system of claim 21, further comprising an enciphering algorithm embedded within said first signal processing circuit for enciphering said processed communication signals.	"signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51 "enciphering algorithm" Claims 10, 26, 45, 51	Please see above, Claims 1 and 10	Please see above, Claims 1 and 10	
43. A communications controller circuit for privately communicating communication signals over a wireless communications network, comprising: a signal processing circuit within said communications controller circuit for processing communications signals	"communications controller circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51 "signal processing circuit" Claims 1, 10, 21,	Please see above, Claim 1	Please see above, Claim 1	

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
to form processed communication signals and further for enciphering said processed communication signals; and a transceiver associated with said communications controller circuit for transmitting said enciphered and processed communication signals from said communications controller circuit.	22, 24, 26, 43-46, 51 "processing (the) … communication(s) signals" Claims 1, 10, 21, 43, 51 "enciphering (the) (said) processed communication signals" Claims 1, 10, 21, 26, 43, 45, 51			

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
44. The controller circuit of claim 43, wherein said signal processing circuit comprises a digital signal processing circuit.	"signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51	Please see above, Claim 1	Please see above, Claim 1	
45. The controller circuit of claim 43, further comprising an enciphering algorithm embedded within said signal processing circuit for enciphering said processed communication signals.	"signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51 "enciphering algorithm" 10, 26, 45, 51	Please see above, Claims 1 and 10	Please see above, Claims 1 and 10	

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
46. The controller circuit of claim 45, further comprising a deciphering algorithm within said signal processing circuit for deciphering processed communication signals received from a second communications controller circuit.	"signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51	Please see above, Claim 1	Please see above, Claim 1	
46. The controller circuit of claim 45, further comprising a deciphering algorithm within said signal processing circuit for deciphering processed communication signals received from a second communications controller circuit.	"deciphering algorithm" Claim 46	a prescribed set of well-defined rules or processes for the solution of a problem in a finite number of steps <u>Intrinsic Evidence:</u> '555 patent: Col. 1:28-30; Col. 7:45-61; Col. 8:53-54; Col. 10:56-63; Fig. 6 <u>Extrinsic Evidence:</u> See, e.g., "decipher" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 359 see, e.g., "algorithm" in Newton's Telecom Dictionary, 10th Edition,	a series of steps for decrypting signals <u>Extrinsic Evidence:</u> <u>IEEE Standard Dictionary of Electrical and Electronic Terms</u>, The Institute of Electrical and Electronics Engineers, Inc., 1988, p. 29, defining "Algorithm" as "(1) (general) - A prescribed set of well-defined rules or processes for the solution of a problem in a finite number of steps. (2) (software) - (1) a finite set of well-defined rules for the solution of a problem in a finite number of steps; (2) a finite set of well-defined rules which gives a sequence of operations for performing a	"a prescribed set of well defined rules or processes for decrypting signals

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
		1996, Flatiron Publishing, Inc., p. 66	specific task." Newton's Telecom Dictionary, 10th Edition, 1996, Flatiron Publishing, Inc., p. 66, defining "algorithm" as "[a] prescribed finite set of well defined rules or processes for the solution of a problem in a finite number of steps." Newton's Telecom Dictionary, 18th Edition, 2002, CMP Books. p. 102, defining "block cipher" as "A digital encryption method which ciphers long messages by segmenting them into blocks of fixed length, prior to encryption. Each block, which typically is 64 bits in length, is encrypted individually. The blocks may be sent as individual units, or they may be linked in a method knows [sic] as Cipher-Block-Chaining."	
51. A communications controller circuit for privately communicating communication signals	"communications controller circuit"	Please see above, Claims 1 and 10	Please see above, Claims 1 and 10	

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
over a wireless communications network, comprising: a signal processing circuit within said communications controller circuit for processing communications signals to form processed communication signals and further for enciphering said processed communication signals; and a transceiver associated with said communications controller circuit for transmitting said enciphered and processed communication signals from said communications controller circuit; wherein said signal processing circuit	Claims 1, 10, 21, 22, 24, 26, 43-46, 51 "signal processing circuit" Claims 1, 10, 21, 22, 24, 26, 43-46, 51 "processing (the) … communication(s) signals" Claims 1, 10, 21, 43, 51 "enciphering (the) (said) processed communication signals"			

'555 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
comprises circuitry and instructions for enciphering said processed communication signals in said signal processing circuit by programmably selecting an enciphering algorithm.	Claims 1, 10, 21, 26, 43, 45, 51 "programmably selecting an enciphering algorithm" Claims 10, 51 "enciphering algorithm" Claims 10, 26, 45, 51			

'394 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
11. An apparatus comprising a plurality of signal processors, a master processor, and a plurality of memories, each signal processor having write access at any time to only a particular one of said memories and read access at any time to any of said memories, wherein at least one of said signal processors in said plurality operates independently of other signal processors in said plurality of signal processors, and wherein said signal processors provide a respective indication signal to said master processor so as to notify said master processor that newly-written-in-data can be obtained from one or more of said plurality of	"signal processor" Claim 11	processor for executing instructions to perform programmed tasks Intrinsic Evidence: '394 patent: Col. 1:23-28; Col. 2:17-21; Col. 2:23-27; Col. 3:30-56; Col. 5:60 - Col. 6:20; Fig. 1a, Fig. 1b	a programmable device that interprets and executes instructions for performing signal processing Intrinsic Evidence: '394 patent: Abstract; Col. 1, ll. 23-27; Col. 2, ll. 5-8, 17-19; Col. 3, ll. 30-56; Col. 4, l. 45 - Col. 5, l. 4; Col. 5, l. 60 - Col. 6, l. 20. Intrinsic Evidence from the '394 File History: '394 Patent File History, "Amendment" (Aug. 26, 1997) at 2, 4. Extrinsic Evidence: "3.1731 processor. (1) A device that interprets and executes instructions, consisting of at least an instruction control unit and an arithmetic unit." IEEE Standard Glossary of Computer Hardware Terminology, IEEE Std. 610-10-1994, The Institute of Electrical and Electronics Engineers, Inc., 1994. "This two-part paper explores the	Programmable device that interprets and executes instructions for performing signal processing

'394 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
memories.			architectural features of single-chip programmable digital signal processors (DSPs)... Programmable DSPs are specialized microcomputers for real-time number crunching. Target applications require extensive arithmetic computation, usually with hard real-time constraints." E. A. Lee, Programmable DSP architectures: Part I, *IEEE ASSP Mag.,* pp. 4-19, Oct. 1988. *"Processor, P.* A component that is capable of interpreting a program in order to execute a sequence of operations." Siework, Bell, Newel, Computer Structures Principles and Examples, *McGraw Hill Computer Science Series,* New York, 1982, p. 18. IEEE Standard Dictionary of Electrical and Electronic Terms, 6th ed., p. 823, defining "processor" as "a device that interprets and executes instructions…."	

'394 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
11. An apparatus comprising a plurality of signal processors, a master processor, and a plurality of memories, each signal processor having write access at any time to only a particular one of said memories and read access at any time to any of said memories, wherein at least one of said signal processors in said plurality operates independently of other signal processors in said plurality of signal processors, and wherein said signal processors provide a respective indication signal to said master processor so as to notify said master processor that newly-written-in-data can be obtained from one or more of said plurality of memories.	"master processor" Claim 11	general purpose processor not under control of a signal processor Intrinsic Evidence: '394 patent: Col. 2:5-8; Col. 2:15-18; Col. 9:63-67; Col. 11:63-67; Fig. 1a; Fig. 1b; Amendment 8/26/1997, p. 5	a general purpose microprocessor, not under the control of a signal processor, that controls the apparatus <u>Intrinsic Evidence:</u> '394 patent: Col. 1, ll. 55-60; Col. 2, ll. 5-32; Col. 3, ll. 21-29; Col. 13, ll. 4-8. <u>Intrinsic Evidence from the '394 File History:</u> '394 Patent File History, "Amendment" (Aug. 26, 1997) at 2, 4.	General purpose processor not under control of a signal processor
11. An apparatus comprising a plurality of signal processors, a master	"each signal processor having write	each of said plurality of signal processors being able to write to only a particular memory	each signal processor can always: (1) write without delay to only its exclusive memory; and (2) read	each signal processor can always: (1) write without delay to only its exclusive memory; and (2) read

'394 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
processor, and a plurality of memories, each signal processor having write access at any time to only a particular one of said memories and read access at any time to any of said memories, wherein at least one of said signal processors in said plurality operates independently of other signal processors in said plurality of signal processors, and wherein said signal processors provide a respective indication signal to said master processor so as to notify said master processor that newly-written-in-data can be obtained from one or more of said plurality of memories.	access at any time to only a particular one of said memories and read access at any time to any of said memories" Claim 11	location, and said each of said plurality of signal processors being able to read from said particular memory location as well as other respective particular memory locations <u>Intrinsic Evidence:</u> '394 patent: Col. 2:27-33; Col. 4:1-17; Col. 4:57-59; Col. 5:1-4; Col. 5: 49-52; Col. 6:65-67; Col. 7:1-7 <u>Extrinsic Evidence:</u> See "[read/write] access" in the Microsoft Press Computer Dictionary, 1991, Microsoft Press, p. 7 See "memory" "storage" and "storage location" in The New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Edition, IEEE Std 100-1992, pp. 797, 1294-96	without delay from any of the memories <u>Intrinsic Evidence from the '394 File History:</u> '394 Patent File History, "Amendment and Request for Reconsideration Under 37 C.F.R. § 1.111" (Jan. 11, 1996) at 3-4, ***et al.*** '394 Patent File History, "Amendment and Request for Reconsideration Under 37 C.F.R. § 1.111" (Jan. 11, 1996) at 5, ***et al.*** '394 Patent File History, "Examiner's Action" (April 1, 1996) at 3, ***et al.*** '394 Patent File History, "Office Action" (Oct. 16, 1995). See Dann '373 at Col. 4, l. 59 - Col. 5, l. 40. Dann '373 Col. 2, ll. 60-64 and Col. 5, ll. 14-30. <u>Intrinsic Evidence from the '394 Specification</u>: '394 patent: Col. 5, ll. 5-32; Fig. 1b.	without delay from any of the memories

'394 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
			Extrinsic Evidence: "anytime... at any time whatever: under any circumstances." Webster's Third New International Dictionary, Unabridged. Merriam-Webster, 2002. http://unabridged.merriam-webster.com (Jan. 8, 2009).	
11. An apparatus comprising a plurality of signal processors, a master processor, and a plurality of memories, each signal processor having write access at any time to only a particular one of said memories and read access at any time to any of said memories, wherein at least one of said signal processors in said plurality operates independently of other signal processors in said plurality of signal processors, and wherein said signal processors provide a respective indication signal to said master processor so as to	"at least one of said signal processors in said plurality operates independently of other signal processors" Claim 11	one (1) or more of the signal processors of said plurality of signal processors executes instructions autonomously from another one of said signal processors Intrinsic Evidence: '394 patent: Abstract; Col. 3:30-56; Col. 3:57 - Col. 4:29; Col. 5:60 - Col. 6:20; Col. 9:56-67; Amendment 01/11/1996, p. 2; Amendment 01/25/1996, pp. 3-4 Extrinsic Evidence: See "independent" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 690	at least one signal processor can operate without being interrupted by any of the two or more other signal processors Intrinsic Evidence: '394 patent: Abstract; Col. 3, ll. 44-51; Col. 5, ll. 12-16; Col. 10, ll. 56-62; claim 11. Extrinsic Evidence: "independent... 1: not dependent: as a (1): not subject to control by others : not subordinate : SELF-GOVERNING, AUTONOMOUS, FREE." Webster's Third New International Dictionary, Unabridged. Merriam-Webster, 2002. http://unabridged.merriam-	at least one signal processor can operate without being interrupted by any of the two or more other signal processors

'394 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
notify said master processor that newly-written-in-data can be obtained from one or more of said plurality of memories.		See "plurality" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 1053	webster.com (Jan. 8, 2009).	
11. An apparatus comprising a plurality of signal processors, a master processor, and a plurality of memories, each signal processor having write access at any time to only a particular one of said memories and read access at any time to any of said memories, wherein at least one of said signal processors in said plurality operates independently of other signal processors in said plurality of signal processors, and wherein said signal processors provide a respective indication signal to said master processor so as to notify said master	"respective indication signal" Claim 11	a respective signal to said master processor so as to indicate to said master processor <u>Intrinsic Evidence:</u> '394 patent: Col. 4:31-40 Col. 8:42-57; Amendment 8/26/1997, p. 5; Fig. 1a; Fig 1b <u>Extrinsic Evidence:</u> See "respective" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 1162 See, "signal" in the Microsoft Press Computer Dictionary, 1991, Microsoft Press, p. 317	a signal generated by a signal processor that instructs the master processor to read that signal processor's exclusive memory <u>Intrinsic Evidence:</u> '394 patent: Col. 4, ll. 36-40; Col. 5, ll. 5-24, 26-32; Col. 6, ll. 58-62; Col. 12; ll. 66-67; Col. 13, ll. 4-8; Fig. 1b. <u>Intrinsic Evidence from the '394 File History:</u> '394 Patent File History, "Amendment and Request for Reconsideration Under 37 C.F.R. § 1.111" (Jan. 11, 1996).	No construction necessary

'394 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
processor that newly-written-in-data can be obtained from one or more of said plurality of memories.				
11. An apparatus comprising a plurality of signal processors, a master processor, and a plurality of memories, each signal processor having write access at any time to only a particular one of said memories and read access at any time to any of said memories, wherein at least one of	"wherein said signal processors provide a respective indication signal to said master processor so as to notify said master processor that newly-written-	wherein said signal processors provide a respective signal to said master processor so as to indicate to said master processor that a corresponding signal processor has written readable data <u>Intrinsic Evidence:</u>	Defendants contend that the construction of this phrase is unnecessary in light of Defendants' proposed construction for the claim term above.	No construction necessary

'394 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
said signal processors in said plurality operates independently of other signal processors in said plurality of signal processors, and wherein said signal processors provide a respective indication signal to said master processor so as to notify said master processor that newly-written-in-data can be obtained from one or more of said plurality of memories.	in data can be obtained" Claim 11	'394 patent: Col. 4:31-40; Col. 8: 42-57; Amendment 8/26/1997, p. 5; Fig. 1a; Fig 1b Extrinsic Evidence: See "respective" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 1162 See, "signal" in the Microsoft Press Computer Dictionary, 1991, Microsoft Press, p. 317		
12. The apparatus recited in claim 11, wherein said plurality of memories comprise respective portions of a same memory.	"respective portions of a same memory" Claim 12	allocated corresponding memory locations within a memory unit Intrinsic Evidence: '394 patent: Col. 5:5-32 Extrinsic Evidence: See "respective" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 1162 See "portion" in The American	Defendants contend that this claim term is more appropriately construed in the context of the larger claim phrase in which it appears, below.	No construction necessary

'394 Claims	Term and Claim(s) in which it appears	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Construction
		Heritage College Dictionary, 1993, Houghton Mifflin, p. 1066		
12. The apparatus recited in claim 11, wherein said plurality of memories comprise respective portions of a same memory.	"said plurality of memories comprise respective portions of a same memory" Claim 12	said plurality of memories comprise allocated corresponding memory locations of a single memory device Intrinsic Evidence: '394 patent: Col. 5:5-32 Extrinsic Evidence: See "respective" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 1162 See "portion" in The American Heritage College Dictionary, 1993, Houghton Mifflin, p. 1066 See "memory" "storage" and "storage location" in The New IEEE Standard Dictionary of Electrical and Electronics Terms, Fifth Edition, IEEE Std 100-1992, pp. 797, 1294-96	the plurality of memories are respective blocks of a single memory device Intrinsic Evidence: '394 patent: Col. 5, ll. 5-32; Fig. 1b. Extrinsic Evidence: "memory... 6a: a component in an electronic computing machine (as a computer) in which information (as data or program instructions) may be inserted and stored and from which it may be extracted when wanted." Webster's Third New International Dictionary, Unabridged. Merriam-Webster, 2002. http://unabridged.merriam-webster.com (Jan. 8, 2009).	said plurality of memories comprise allocated corresponding memory locations of a single memory device